

Multicore Computer Architecture - Storage and Interconnects

Introduction and overview of the course



NPTEL Online Course Multi-Core Computer Architecture - Storage and Interconnects Dr. John Jose IIT Guwahati

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Course Objective

- ❖ **Learn** and **appreciate** computer architecture with an emphasis on system design, performance and analysis.
- ❖ **Elevate** computer architecture related discussions and thoughts to performance improvement of storage and interconnect mechanisms in multi-core systems.
- ❖ **Understand** and **analyze** events happening at hardware level with the help of open source simulators.
- ❖ **Enable** exploration of future directions in computer architecture research.

Focus Area of the Course

- ❖ Processor design trends - instruction pipeline concepts, out-of-order execution, introduction to superscalar processors.
- ❖ Cache memory concepts and optimization techniques, DRAM organization, design concepts in memory controllers, principles and practices of Network on Chips.
- ❖ Performance improvement techniques for recent multicore processors at the level of caches and interconnects.
- ❖ Hands on experience in system design and analysis with the help of open source computer architecture simulator gem5.

Syllabus & Course Plan

❖ **Week 1: Pipelined instruction execution principles**

Instruction execution fundamentals, concept of memory and addressing. Performance measurement of computer hardware-MIPS, IPC. Speed-up and Amdahl's Law. MIPS instruction set, RISC vs CISC architectures. Concept of instruction pipelining, RISC instruction set, RISC 5 stage pipeline, pipeline hazards, operand forwarding, branch prediction techniques.

Syllabus & Course Plan

❖ Week 2: Cache memory design concepts

Introduction to memory hierarchy, locality of reference, cache memory fundamentals, cache performance parameters. Block level issues -mapping, identification, replacement, write strategy, types of misses-compulsory, capacity, conflict misses. Basic cache optimizations by adjusting cache size, block size, associativity.

Syllabus & Course Plan

❖ **Week 3: Advanced cache optimizations**

Advanced cache optimizations-way prediction, pipelined and non-blocking caches, multi-banked caches, critical word first, early restart approaches, compiler optimizations.

Syllabus & Course Plan

❖ **Week 4: Advanced cache optimizations and virtual memory concepts**

Advanced cache optimizations- hardware pre-fetching, write buffer merging. Virtual memory concepts, paging and segmentation, address translations using TLB and page tables.

Introduction to gem5 simulator. Overview of simulator based assignments.

Syllabus & Course Plan

❖ Week 5 : DRAM technology

Introduction to DRAM organization- DIMMs, channels, ranks, banks, rows, columns, sense amplifiers and device control logic .

Memory controllers- DRAM timing and signaling, access protocols, commands, bank and rank conflicts, DRAM refresh circuitry and power managements schemes, DRAM scheduling.

Syllabus & Course Plan

❖ **Week 6: Tiled Chip Multicore Processors & Network-On-Chip**

Introduction to TCMP, multicore processors, communication issues in TCMPs, role of NoCs, topology schemes, routing – deterministic and adaptive routings, input and output selection strategies, congestion managements with selection strategies.

Syllabus & Course Plan

❖ Week 7: Network-On-Chip Architectures

NoC router micro architecture, input buffered routers, flow control techniques, virtual channels and deadlock management, allocators and arbiter algorithms for crossbar switch.

Introduction to deflection routers, minimally buffered router designs, compression and prefetch aware NoC designs.

Syllabus & Course Plan

❖ **Week 8: QoS for TCMPs at storage and interconnect levels.**

Need for QoS at on-chip shared resources like caches, NoC and memory controllers, cache management techniques for multi-core systems, introduction to wireless and optical NoCs.

Discussion of selected papers published in ISCA, HPCA, MICRO, DAC, DATE, NOCS and ICCD conferences, future road map ahead for computer architecture research.

Reference Books

- ❖ **Computer Architecture-A Quantitative Approach** (5th edition), John L. Hennessy, David A. Patterson, Morgan Kaufman.
- ❖ **Advanced Computer Architectures-A Design Space Approach**, Dezsó Sima, Terence Fountain, Peter Kacsuk, Pearson.
- ❖ **Computer Architecture-Pipelined and Parallel Processor Design**, Michael J. Flynn, Narosa Publishing House.
- ❖ **Memory System-Cache, DRAM and Disk**, Bruce Jacob, Spencer W. Ng, David T. Wang, Morgan Kaufman.

Comfort vs Discomfort Zone

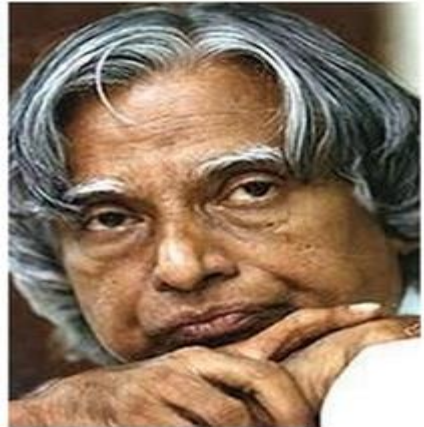
There are two roads in life: a high road and a low road.

The high road is harder, but it takes you somewhere worth going.

The low road is easy, but it's circular. You eventually find yourself back where you started.

Your life won't get better and you won't get better on the low road.

—Dr. A.P.J. Abdul Kalam



This course is for those who are willing to take up the risk (enjoy the beauty) in understanding how a computer work by digging deep into its architecture.

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It is not the destination (final grade), but the unique experience in the journey (lectures and discussions) that is important, So enjoy the ride !!!

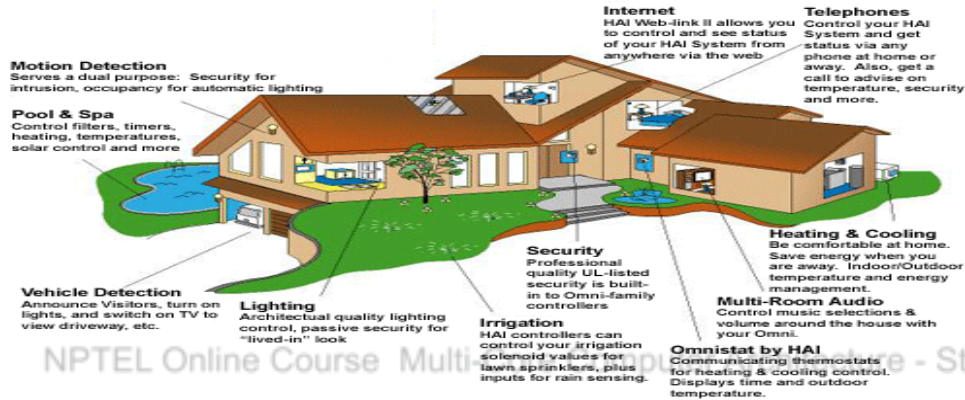
Role of computer architects

Applications and hand held devices are parcel of our day to day life



What are the hardware architectural support needed for these applications ?

Smart Homes



THE SMART HOME



- Alarm
- Cameras
- Text/Email Alerts
- Remote Access to Lights & Locks



- Networking
- Concierge Service
- Remote Access Via SMART Panel to Home Systems

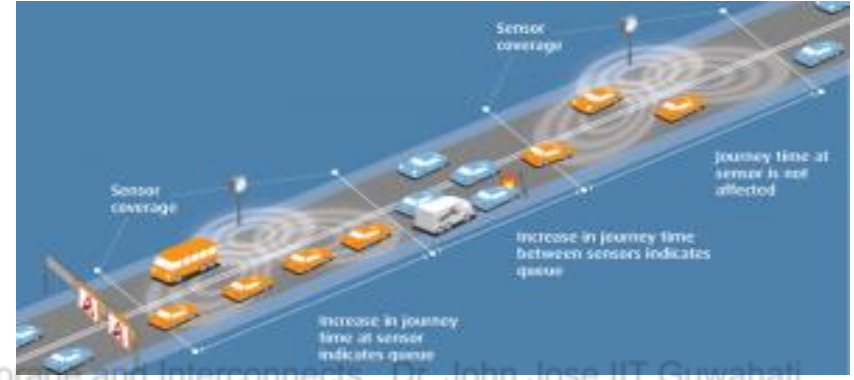


- Surround Sound
- Whole House Audio
- Video Distribution
- Phone/Tablet as Home A/V "Remote Control"

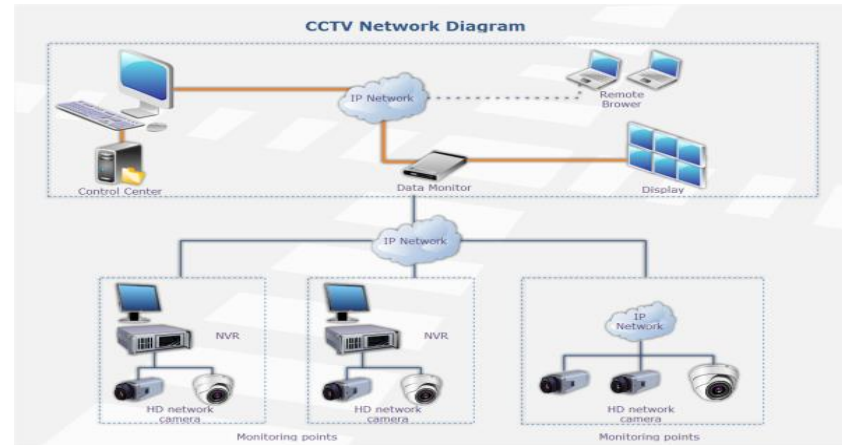
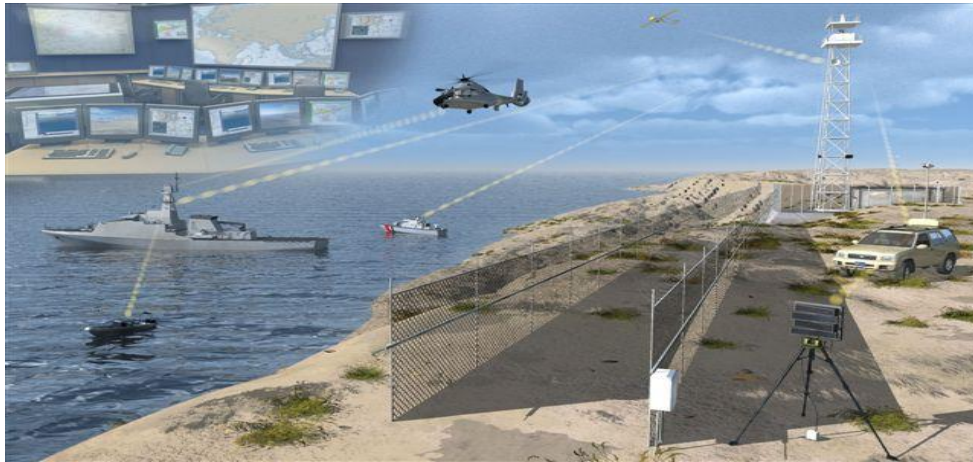


- A/C Control
- Fire/ Carbon Monoxide/Water Email and Text Alerts

Driverless Vehicles



Video Surveillance



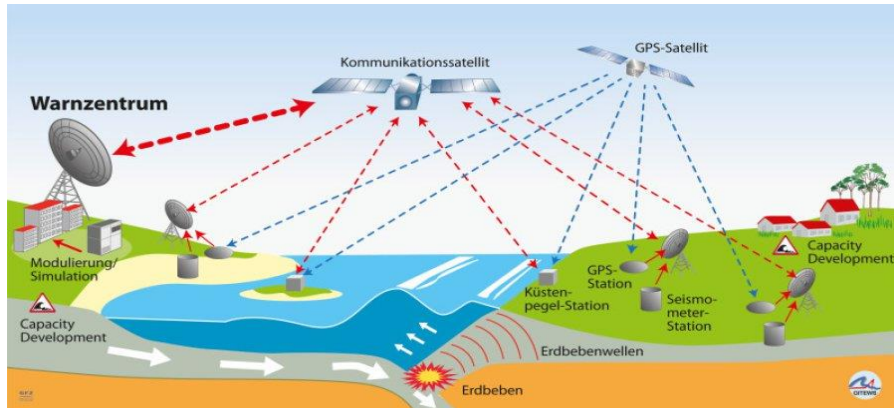
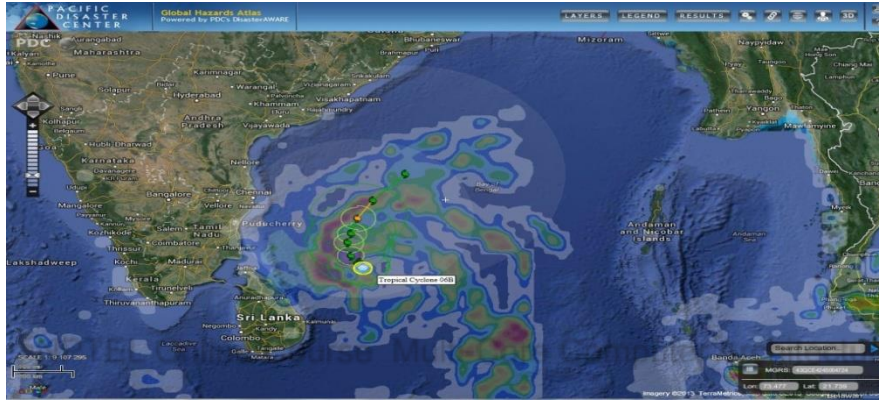
Smart Health Care



NPTEL Course Content: Multi-Core Computer Architecture - Storage and Interconnects Dr. John Jose IIT Guwahati



Weather Forecasting

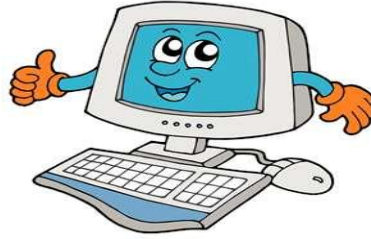


Smart Life and Health Ahead

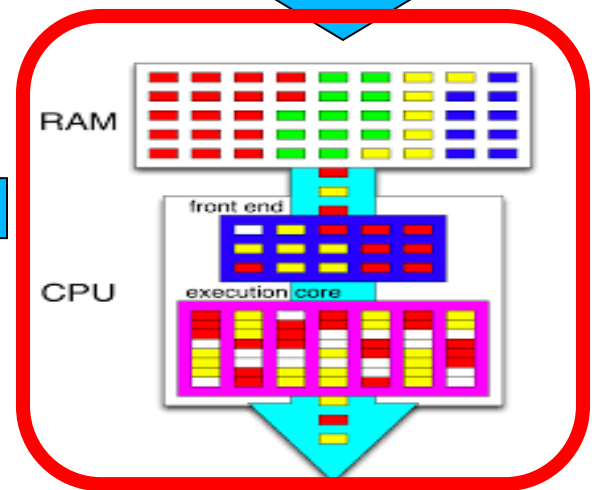
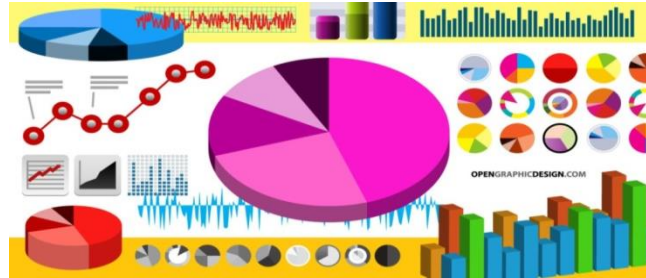


SmartPlanet

How is this all done ?

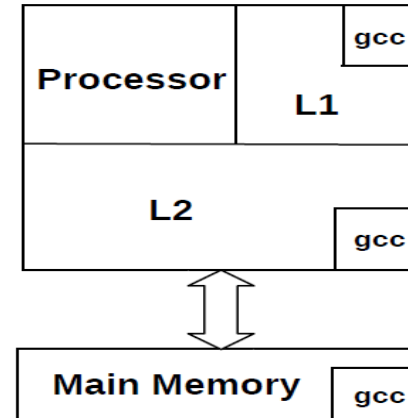
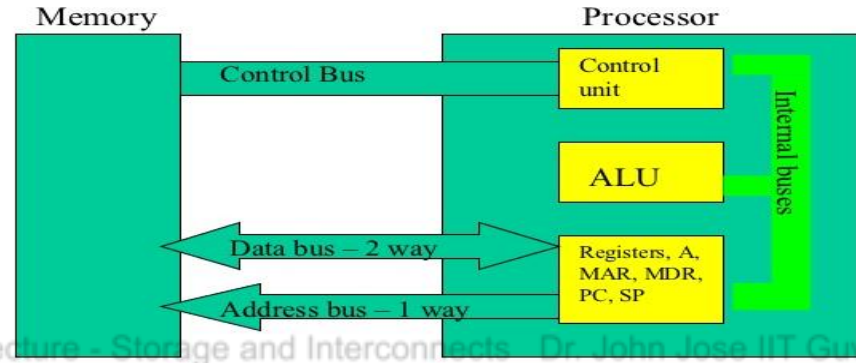


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Processor Memory Interaction

<i>Instruction Fetch</i>
<i>Instruction Decode</i>
<i>Operand Fetch</i>
<i>Execute</i>
<i>Result Store</i>
<i>Next Instruction</i>



**THANK
YOU!**

**FOR
YOUR
PRESENCE**

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